REMARKS

Claims 1-9 are pending in the application. By this Amendment, claim 1 has been amended. No new matter has been added. It is respectfully submitted that this Amendment is fully responsive to the Office Action dated October 4, 2007.

As to the Merits:

As to the merits of this case, the Examiner now relies on the newly cited reference of Suzuki (USP 6,975,357) in setting forth the following rejections:

claims 1-4, 6, 7 and 9 stand rejected under 35 U.S.C. §102(e) as being anticipated by Suzuki; and

claims 5 and 8 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Suzuki in view of Kochi.

Each of these rejections is respectfully traversed.

Claim 1, as amended, now calls for *a vertical scanning circuit in a pixel reset period concurrently selects the pixels of n rows (n being an integer of 2 or more) at a first timing to concurrently effect only a reset operation of the pixels of the n rows thereof and selects at a second timing subsequent to the first timing the pixels of n rows of the address different from the rows selected at the first timing to concurrently effect only a reset operation of the pixels of the n*

rows thereof, reset operation in this manner being repeated to effect a reset operation of all pixels.

The invention relates to the resetting of XY-addressing type solid-state imaging apparatus, where, in a pixel reset period, the pixels of n rows are concurrently selected at a first timing by a vertical scanning circuit to simultaneously and collectively effect a reset operation of the pixels of the n rows thereof, and the pixels of n rows having the address different from the first timing are concurrently selected at a second timing subsequent to the first timing to simultaneously and collectively effect a reset operation of the pixels of the n rows thereof. By repeating reset operation in this manner, all pixels are reset.

In particular, as shown in the timing chart of Fig. 6 of the present application, a reset operation of all pixels is effected by pulse ΦRS from a vertical scanning circuit in the pixel reset period, and, after passage of accumulation period, signals are read out from the pixels by pulse ΦHm from a horizontal scanning circuit in a signal output period. Therefore, the reset operation and the read operation are effected in separate periods from each other and by different scanning circuits from each other.

With such reset method, the pixels of a plurality of rows can be concurrently reset to make it possible to reduce time for resetting all pixels, and reset time of all pixels without

depending on the number of pixels can be obtained by adjusting the number of pixel rows to be concurrently reset.

Suzuki, on the other hand, concurrently selects two rows by a vertical scanning circuit, and, for the pixels of the selected two rows, readout of pixel signals is sequentially effected column by column in the horizontal direction by horizontal scanning pulse ΦHm from a horizontal scanning circuit. A reset operation of the pixels is then effected by readout of pixel signals by such horizontal scanning pulse ΦHm.

With regard to the applied reference of Suzuki, the Examiner asserts on page 3 of the Action that such reference discloses:

> vertical scanning circuit (3) concurrently selects the pixels of n rows (ΦV1η and ΦV2*η +1*, Fig. 11) at a first timing to concurrently effect a reset operation (through the reset transistor 16, Fig. 6) of the pixels of the n rows thereof and selects at a second timing (after 1V period, Fig. 11) subsequent to the first timing (at time=t1, Fig. 2) the pixels of n rows of the address different from the rows selected at the first timing (ΦV1η +2 and ΦV2*η* + 3, Fig. 11) to effect a reset operation of the pixels of the n rows thereof, reset operation in this manner being repeated to effect a reset operation of all pixels (col. 6, lines 14-53).

It is noted that Suzuki discloses that the first vertical scan pulse ΦV1*n* and the second vertical scan pulse ΦV2*n*+1 are output from the first vertical scan circuit 30 and the second vertical scan circuit 31 respectively at a time t1 by the vertical scan operation of the first and second vertical scan circuits 30, 31, as shown in Figs. 2, 3 and 11.

However, it is submitted that neither of the first vertical scan pulse ΦV1*n* or the second vertical scan pulse ΦV2*n*+1 reset the reset transistor 16.

Instead, according to Suzuki, since "when the horizontal scan pulse ΦHm-1 is output from the horizontal scan circuit 29 and applied to a horizontal selection line 24*m*-1 on the (m-1)-th column, the reset transistor 16 of the pixel of the m-th column is set to ON state, whereby the floated diffusion area FD is reset to the power source VDD through the reset transistor 16."[1]

In addition, Suzuki also discloses that "when the pixels (m,n), (m,n+i) are selected, the pixels (m+1, n), (m+1, n+i) of the next column are reset by the horizontal scan pulse ΦHm." [2]

Moreover, as shown in the timing chart of the horizontal scan operation in Fig. 3, the horizontal scan pulse ΦHm-1 which resets the reset transistor 16 of the pixel of the m-th column and the horizontal scan pulse ΦHm which resets the reset transistor 16 of the pixel of the m+1th column are clearly not performed at the same time.

In other words, in Suzuki, the reset operation of pixels is effected at the same time of reading pixel signals by the horizontal scanning circuit. Accordingly, it is clear that Suzuki is

[1] Please see col. 5, lines 25-30 of Suzuki.

[2] Please see col. 6, lines 7-9 of Suzuki.

unlike the invention of the present case where, in a pixel reset period, n rows are concurrently selected at a first timing and are simultaneously and collectively reset only with a vertical scanning circuit, and n rows different from those of the first timing are concurrently selected at a second timing subsequent to the first timing and are simultaneously and collectively reset, and such reset operation is repeated to effect the reset operation of all pixels.

Accordingly, it is submitted that Suzuki fails to disclose or fairly suggest the features of claim 1 concerning *a vertical scanning circuit in a pixel reset period concurrently selects the pixels of n rows (n being an integer of 2 or more) at a first timing to concurrently effect only a reset operation of the pixels of the n rows thereof and selects at a second timing subsequent to the first timing the pixels of n rows of the address different from the rows selected at the first timing to concurrently effect only a reset operation of the pixels of the n rows thereof, reset operation in this manner being repeated to effect a reset operation of all pixels.*

In view of the aforementioned amendments and accompanying remarks, Applicants submit that the claims, as herein amended, are in condition for allowance. Applicants request such action at an early date.

If the Examiner believes that this application is not now in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney to arrange for an interview to expedite the disposition of this case.

If this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees that may be due with respect to this paper may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

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